

JEDEC STANDARD

Method for Repetitive Inductive Load Avalanche Switching

JESD24-8

AUGUST 1992 (Reaffirmed: OCTOBER 2002)

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or call (703) 907-7559 or www.jedec.org

Published by
©JEDEC Solid State Technology Association 2003
2500 Wilson Boulevard
Arlington, VA 22201-3834

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications or call Global Engineering
Documents, USA and Canada 1-800-854-7179, International (303) 397-7956

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

Organizations may obtain permission to reproduce a limited number of copies
through entering into a license agreement. For information, contact:

JEDEC Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
or call (703) 907-7559

METHOD FOR REPETITIVE INDUCTIVE LOAD AVALANCHE SWITCHING

(From Council Ballot JCB-91-51 formulated under the cognizance of JC-25 Committee on Transistors)

1. PURPOSE

The purpose of this test method is to determine the repetitive inductive avalanche switching capability of power devices.

2. SCOPE

This method is intended as an endurance test for any power switching device designed and specified with repetitive avalanche capability.

3. CIRCUITRY

The basic circuit is shown in Figure 1. The circuit shall be designed so that all stray reactances are held to a minimum. The inductor, L shall be of a fast response type.

4. DEFINITIONS

The following terms and symbols apply to this test method:

T_J	-	Junction temperature
$T_{J(max)}$	-	The maximum specified junction temperature
$R_{\theta JC}$	-	Thermal resistance from the junction to the case
L	-	Load inductance per DUT
E_{AR}	-	Repetitive avalanche energy, minimum
I_{AR}	-	Peak repetitive avalanche current, maximum
E_{on}	-	On state energy
f	-	frequency

T_C	-	Case temperature
P_D	-	Power dissipation of device
$V_{(BR)}$	-	Breakdown or avalanche voltage of device
V_{DD}	-	Power supply voltage
DUT	-	Device under test
R_S	-	Stray circuit resistance
t_{av}	-	Time in avalanche

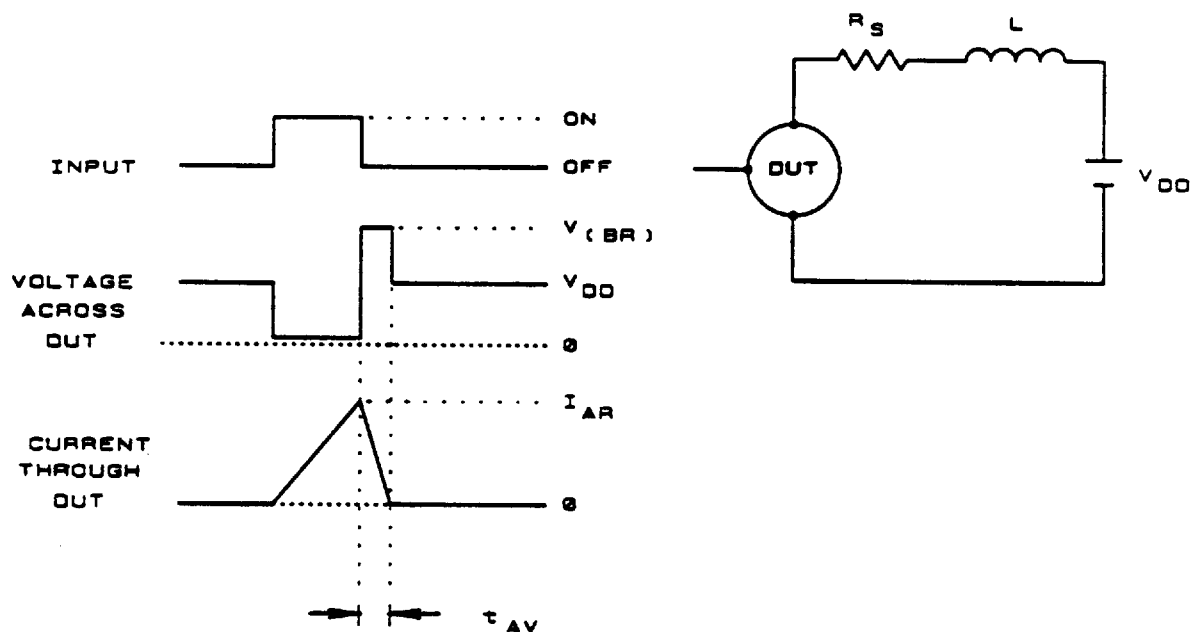


Figure 1
Basic Circuit

5. METHOD

- (a) The DUT must be screened prior to avalanche and meet all specified parameters.
- (b) The energy delivered to the DUT can be calculated as follows:

$$(1) \quad E_{AR} = \frac{L * I_{AR}^2 * V_{(BR)}}{2 [V_{(BR)} - V_{DD}]}$$

NOTE: $R_S = 0$, where $V_{(BR)} = LI_{AR}^2/t_{av}$

$$(2) \quad E_{AR} = V_{BR} * I_{AR} (L/R_S) \ln[I_{AR} * R_S / (V_{BR} - V_{DD}) + 1]$$

NOTE: $R_S = 0$

- (c) The actual energy delivered to the DUT can vary depending on the real value of R_S . Since this resistance is test circuit dependant, the actual energy delivered must be verified by observing waveforms of the voltage across the DUT and current through the DUT waveforms (Refer to Figure 1). Record the $V_{(BR)}$, I_{AR} and t_{av} .

$$(3) \quad E_{AR} = (1/2) (V_{BR} * I_{AR} * t_{AV}). \text{ (per Figure 1)}$$

If this empirically derived value is not greater than or equal to the specified minimum E_{AR} value the circuit must be compensated until it is.

- (d) T_j during the test must be held constant to $T_j(\text{max}) + 0 - 10^\circ\text{C}$, based on the case temperature of the DUT and $R_{\theta JC}$ or the junction temperature sensitive parameter. The power dissipated in the DUT equal to the sum of the on energy and the avalanche energy multiplied by the frequency. The E_{on} in most cases can be neglected.

$$(4) \quad \text{So: } P_D = F * (E_{AR} + E_{on})$$

$$(5) \quad T_J = P_D * R_{\theta JC} + T_C$$

The case temperature of the DUT will be measured at a specified reference point under the heat source. It is also possible to measure the temperature of the heat sink at a specified reference point provided that an accurate value of the thermal resistance case-to-heat-sink-reference-point is known. The measured junction temperature based on measurements of a temperature sensitive parameter may also be substituted for the junction temperature calculated from case temperature.

- (e) The DUT will be avalanched for a specified minimum number of pulses at specified conditions. Upon completion the specified device parameters will be tested.

6. SPECIFICATION

The following parameters must be specified:

E_{AR}	=	Repetitive avalanche energy (joules)
I_{AR}	=	Repetitive avalanche current (amperes)
T_J	=	$T_{J(max)} + 0 - 10^{\circ}C$
t_{av}	=	min, max
f	=	Frequency (hertz), minimum
N	=	Minimum number of pulses
V_{DD}	-	Power supply voltage

7. CRITERIA

The DUT must be within all specified parameter limits at the completion of the test. As a minimum $V_{(BR)} \geq$ rated breakdown voltage at applicable leakage currents.

JEDEC